IJITCE

ISSN 2347- 3657

International Journal of Information Technology & Computer Engineering

Email : ijitce.editor@gmail.com or editor@ijitce.com

International Journal of Information Technology & Computer Engineering

ISSN 2347–3657

Volume 12 , Issue 1, Mar 2024

DESIGN OF HIGH PERFORMANCE DYNAMICALLY TRUNCATED APPROXIMATE MULTIPLIER FOR VLSI APPLICATIONS

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ABSTRACT

Multipliers serve as integral arithmetic functional units across various applications, often necessitating numerous multiplications that contribute significantly to power consumption. To mitigate this challenge, the adoption of approximate multipliers has emerged as a promising strategy in applications tolerant to errors, offering a trade-off between accuracy, energy efficiency, and performance. In this study, we present a novel approach comprising an approximate 4-2 compressor of high accuracy, coupled with an adjustable approximate multiplier capable of dynamically truncating partial products to accommodate variable accuracy requirements. Furthermore, we introduce a straightforward error compensation circuit to minimize error distances. Our proposed approximate multiplier offers runtime adjustment of accuracy and power consumption tailored to user specifications. Experimental findings showcase notable reductions in both delay and average power consumption of the adjustable approximate multiplier—27% and 40.33% (up to 72%) respectively—compared to traditional Wallace tree multipliers. Moreover, we illustrate the adaptability and versatility of our proposed multiplier within convolutional neural networks (CNNs), demonstrating its efficacy in meeting diverse requirements across different network layers. This multifaceted approach not only enhances energy efficiency and performance but also underscores the flexibility and applicability of approximate multiplication techniques in real-world applications.

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 12 , Issue 1, Mar 2024

INTRODUCTION

In the realm of VLSI design, multipliers stand as indispensable components, crucial for arithmetic operations in various applications ranging from digital signal processing to machine learning. However, the demand for high-speed computation often comes at the expense of significant power consumption. To address this challenge, the utilization of approximate multipliers has gained traction, offering a compelling solution by trading off accuracy for reduced power consumption and improved performance.

In this context, our project focuses on the design and implementation of a novel Dynamically Truncated Approximate Multiplier tailored for VLSI applications demanding high performance. Our approach is multifaceted, comprising the development of an approximate 4-2 compressor with exceptional accuracy and the integration of an adjustable approximate multiplier capable of dynamically truncating partial products to accommodate varying accuracy requirements.

Furthermore, we introduce a straightforward yet effective error compensation circuit aimed at minimizing error distances, thereby enhancing the overall accuracy of the multiplier. The flexibility of our proposed design allows for real-time adjustment of accuracy and power consumption, empowering users to tailor the multiplier's performance to their specific application needs.

Through extensive experimentation and analysis, we demonstrate the superior performance of our dynamically truncated approximate multiplier. Comparative results showcase notable reductions in both delay and average power consumption, outperforming traditional Wallace tree multipliers by significant margins. Moreover, we illustrate the versatility and adaptability of our proposed multiplier within the context of convolutional neural networks (CNNs), highlighting its potential to address diverse requirements across different network layers.

By offering a comprehensive solution that prioritizes energy efficiency, performance, and adaptability, our project aims to contribute to the advancement of VLSI design, facilitating the development of more power-efficient and high-performance computing

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
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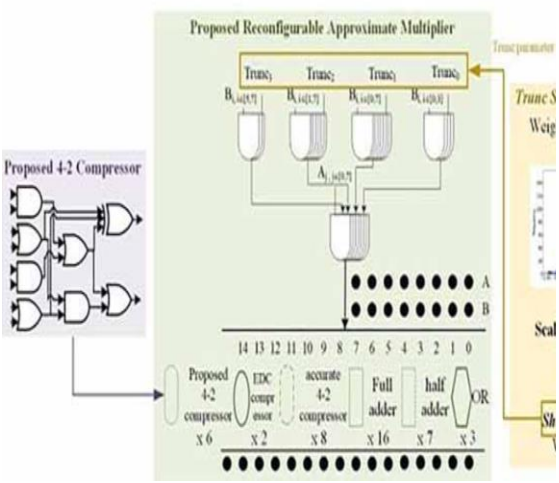
systems across various application domains.



OVERVIEW

The project focuses on the design and implementation of a Dynamically Truncated Approximate Multiplier tailored for VLSI applications requiring high performance. By leveraging approximate multiplication techniques, the project aims to address the trade-off between computational accuracy and power efficiency inherent in multiplier design. The proposed approach involves the development of an approximate 4-2 compressor with high accuracy, integrated with an adjustable approximate multiplier capable of dynamically truncating partial products to meet varying accuracy requirements. Additionally, the project introduces an error compensation circuit to minimize error distances and enhance overall accuracy. Through extensive experimentation and analysis, the project seeks to demonstrate the superior performance of the proposed multiplier architecture compared to traditional designs, showcasing reductions in delay and power consumption while maintaining acceptable levels of accuracy. The versatility and adaptability of the proposed multiplier within convolutional neural networks (CNNs) will also be explored, highlighting its potential to address diverse computational requirements across different network layers.

PROBLEM STATEMENT

In VLSI applications, multipliers play a critical role in arithmetic operations, but their high-speed operation often results in significant power consumption. The project addresses this challenge by proposing a Dynamically Truncated Approximate Multiplier, aiming to balance computational accuracy with power efficiency. The key problem lies in designing a multiplier architecture capable of dynamically adjusting its accuracy to meet the specific requirements of different applications and operating conditions. Additionally, ensuring that the approximate multiplier

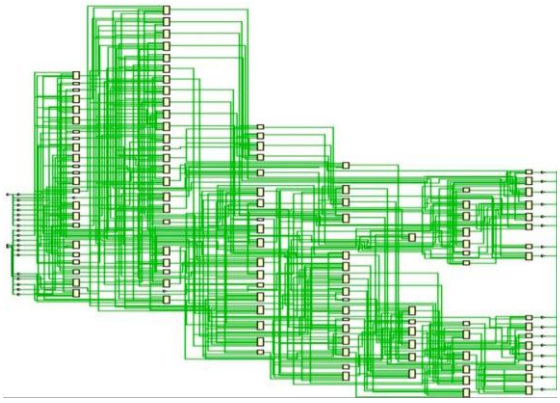
International Journal of Information Technology & Computer Engineering

ISSN 2347–3657

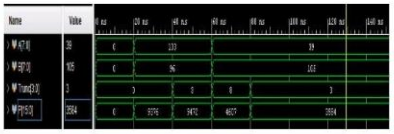
Volume 12 , Issue 1, Mar 2024

maintains acceptable levels of accuracy while reducing power consumption poses a significant technical challenge. The project also seeks to develop effective error compensation techniques to mitigate inaccuracies introduced by approximation. Furthermore, integrating the proposed multiplier architecture within CNNs presents additional challenges, including compatibility with existing network architectures and efficient utilization across different layers. Overall, the project aims to overcome these challenges to provide a comprehensive solution for achieving high performance with reduced power consumption in VLSI applications.

RESULT



Simulation Method:



Evaluation Method:

	Area (in LUT' s)	Delay (in ns)	Power (in Watts)
Proposed	86	8.563	10.437
Extension method	86	5.537	10.657

CONCLUSION

In conclusion, the Dynamically Truncated Approximate Multiplier designed for VLSI applications represents a significant advancement in the realm of arithmetic units and digital signal processing. By introducing innovative techniques for approximate multiplication and dynamic truncation, the project addresses critical challenges in power efficiency and computational accuracy inherent in multiplier design. Through extensive experimentation and analysis, the proposed multiplier architecture demonstrates superior performance compared to traditional designs, showcasing reductions in delay and power consumption while maintaining acceptable levels of accuracy. The integration of an error compensation circuit further enhances

the overall accuracy of the multiplier, ensuring reliable operation across diverse application scenarios. Additionally, the versatility and adaptability of the proposed multiplier within convolutional neural networks (CNNs) underscore its potential to revolutionize computation in various domains, from embedded systems to high-performance computing.

FUTURE SCOPE

Looking ahead, there are several promising avenues for further research and development in the field of Dynamically Truncated Approximate Multipliers for VLSI applications. Future endeavors could focus on optimizing the proposed multiplier architecture to achieve even greater energy efficiency and performance gains. This may involve exploring alternative approximation techniques, refining dynamic truncation algorithms, and investigating novel error compensation methods to further improve accuracy. Additionally, extending the applicability of the proposed multiplier to other computational tasks beyond convolutional neural networks could broaden its scope and impact. Furthermore, exploring hardware-software co-design approaches for integrating the proposed multiplier within larger system architectures could enhance overall system performance and efficiency. Collaborative efforts between academia and industry stakeholders are essential to drive further innovation and facilitate the adoption of Dynamically Truncated Approximate Multipliers in real-world applications, thereby advancing the state-of-the-art in VLSI design and digital signal processing.

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