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Cascaded Multilevel Inverter Based On Switched Capacitor For High Frequency AC Power distribution System

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Abstract:

Compared to low- or medium-frequency distribution, transmission frequencies that are higher show greater benefits in various power applications. In a high-frequency alternating current (HFAC) power distribution system (PDS), the high-frequency inverter acts as the source side. A high-frequency inverter with an easy-to-understand modulation scheme and a simple circuit architecture is difficult to achieve, however. This work presents a new cascaded multilevel inverter that uses switched-capacitor frontends and H-Bridge backends. The switching capacitor frontend expands the voltage range by converting series and parallel connections. As the number of voltage levels increases, the output harmonics and component counting may be greatly decreased. An analog implementation of symmetrical triangular waveform modulation is suggested, which has a low modulation frequency in comparison to conventional multicarrier modulation. Topics covered include topology augmentation, symmetrical modulation, operation cycles, parameter determination, and Fourier analysis. In order to compare the results of the simulation with the prototype, a Matlab/Simulink system is set up with a rated output frequency of 25 kHz.

Topics covered include cascading H-Bridges, symmetrical phaseshift modulation, switching capacitors, multilevel inverters, and high-frequency alternating current (HFAC). I.

INTRODUCTION

High Frequency ac (HFAC) power distribution system (PDS) potentially becomes an alternative to traditional dc distribution due to the fewer components and lower cost. The existing applications can be found in computer [1], telecom [2], electric vehicle [3], and renewable energy microgrid [4], [5]. However, HFACPDS has to confront the challenges from large power capacity, high electromagnetic interference (EMI), and severe power losses [6]. A traditional HFAC PDS is made up of a highfrequency (HF) inverter, an HF transmission track, and numerous voltage-regulation modules (VRM). HF inverter accomplishes the power conversion to accommodate the requirement of point of load (POL). In order to increase the power capacity, the most popular method is to connect the inverter output in series or in parallel. However, it is impractical for HF inverter, because it is complicated to simultaneously synchronize both amplitude and phase with HF dynamics. Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity is easy to be achieved by multilevel inverter with lower switch stress. Nonpolluted sinusoidal waveform with the lower total harmonic distortion (THD) is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of staircase output, thus significantly simplifying the filter design [7].

HF power distribution is applicable for small-scale and internal closed electrical network in electric vehicle (EV) due to moderate size of distribution network and effective weight reduction [8]. The consideration of operation frequency has to make compromise between the ac inductance and resistance [9], so multilevel inverter with the output frequency of about 20 kHz is a feasible trial to serve as power source for HF EV application. The traditional topologies of multilevel inverter mainly are diode-clamped and capacitor-clamped type [10], [11]. The former uses diodes to clamp the voltage level, and the latter uses additional capacitors to clamp the voltage. The higher number of

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voltage levels can then be obtained; however, the circuit becomes extremely complex in these two topologies. Another kind of multilevel inverter is cascaded H-Bridge constructed by the series connection of H-Bridges [12], [13]. The basic circuit is similar to the classical H-bridge DC–DC converter [14].

The cascaded structure increases the system reliability because of the same circuit cell, control structure and modulation. However, the disadvantages confronted by cascaded structure are more switches and a number of inputs. In order to increase two voltage levels in staircase output, an H-Bridge constructed by four power switches and an individual input are needed. Theoretically, cascaded H-Bridge can obtain staircase output with any number of voltage levels, but it is inappropriate to the applications of cost saving and input limitation. A number of studies have been performed to increase the number of voltage levels. A switched-capacitor (SC) based multilevel circuit can effectively increase the number of voltage levels. However, the control strategy is complex, and EMI issue becomes worse due to the discontinuous input current [15]. A single-phase five-level pulsewidth-modulated (PWM) inverter is constituted by a full bridge of diodes, two capacitors and a switch. However, it only provides output with five voltage levels, and higher number of voltage levels is limited by circuit structure [16]. An SC-based cascaded inverter was presented with SC frontend and full bridge backend. However, both complicated control and increased components limit its application [17]. The further study was presented using series/parallel conversion of SC. However, it is inappropriate to the applications with HF output because of multicarrier PWM (MPWM) [18], [19]. If output frequency is around 20 kHz, the carrier frequency reaches a couple of megahertz. Namely, the carrier frequency in MPWM is dozens times of the output frequency. Since the carrier frequency determines the switching frequency, a high switching loss is inevitable for the sake of high-frequency output. A boost multilevel inverter based in partial charging of SC can increase the number of voltage levels theoretically. However, the control strategy is complicated to implement partial charging [20]. Therefore, it is a challenging task to present an SC-based multilevel inverter with highfrequency output, low-output harmonics, and high conversion efficiency [21]. Based on the study situation aforementioned, a novel multilevel inverter and simple modulation strategy are presented to serve as HF power source. The rest of this paper is organized as follows. The discussions of nine-level inverter are presented including circuit topology, modulation strategy, operation cycle, and Fourier analysis. The performance evaluation accomplished by simulation is described in Section III followed by concluding remarks.

II. SC-BASED CASCADED INVERTER WITH NINELEVEL OUTPUT

The proposed circuit is made up of the SC frontend and cascaded H-Bridge backend. If the numbers of voltage levels obtained by SC frontend and cascaded H-Bridge backend are N1 and N2 , respectively, the number of voltage levels is 2× N1×N2+1 in the entire operation cycle.

Circuit Topology

Fig. 1 shows the circuit topology of nine-level inverter (N1 = 2, N2 = 2), where S1, S2, S_ 1 , S_ 2 as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of C1 and C2 . S1a, S1b, S1c, S1d, S2a, S2b, S2c, S2d are the switching devices of cascaded H-Bridge. Vdc1 and Vdc2 are input voltage. D1 and D2 are diodes to restrict the current direction. iout and vo are the output current and the output voltage, respectively. It is worth noting that the backend circuit of the proposed inverter is cascaded H-Bridges in series connection. It is significant for H-Bridge to ensure the circuit conducting regardless of the directions of output voltage and current. In other words, HBridge has four conducting modes in the conditions of inductive and resistive load, i.e., forward conducting, reverse conducting, forward freewheeling, and reverse freewheeling.

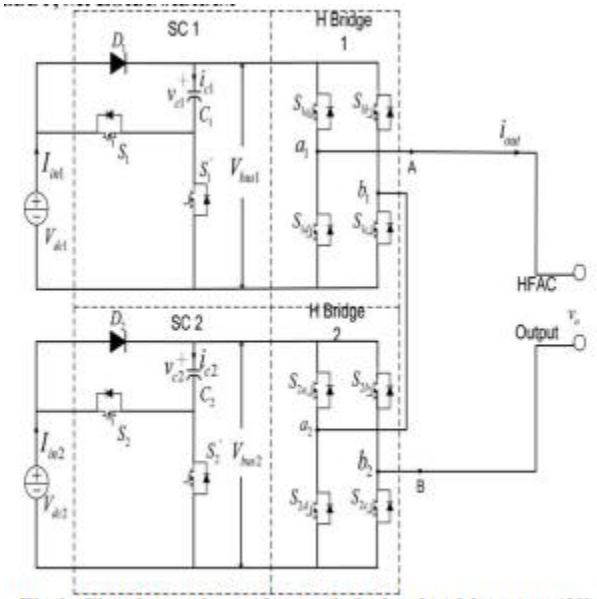

Fig.1. Circuit topology of cascaded nine-level inverter (*N*1 = 2, *N*2 = 2).

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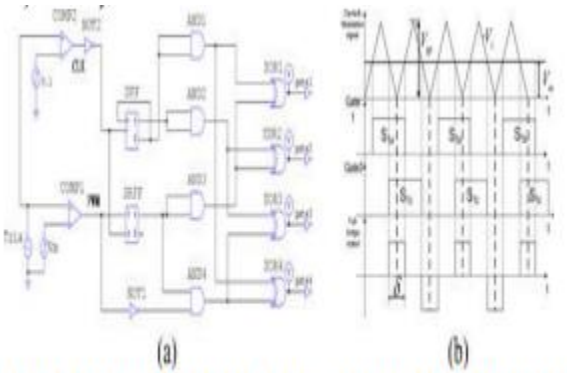

Fig.2. Circuit and operational waveforms of symmetrical PSM. (a) Circuit of symmetrical PSM. (b) Operational waveforms of symmetrical PSM.

Symmetrical Modulation

There are many modulation methods to regulate the multilevel inverter, the popular modulations are the space vector modulation [22], the multicarrier PWM [23], and the selective harmonic elimination [24], [25], sub harmonic pulse width modulation [26], etc. However, most of them greatly increase the carrier frequency that is dozens times the frequency of reference or output. A symmetrical phase-shift modulation (PSM) is introduced into the proposed multilevel inverter. The symmetrical PSM ensures the output voltage of full bridge is symmetrical to the carrier, so voltage levels can be superimposed symmetrically and carrier frequency is twice as that of the output frequency [27]. The structure of symmetrical PSM is shown in Fig. 2(a), and the operational waveform of symmetrical PSM is shown in Fig. 2(b). The logic operations of gate signals are

$$\begin{aligned} gate1 &= XOR\{Q(RS), Q(D)\} \\ gate2 &= XOR\{Q(RS), Q(D)\} \quad (1) \\ gate3 &= XOR\{AND\{Q(RS), NOT(PWM)\}, Q(D)\} \\ gate4 &= XOR\{AND\{Q(RS), NOT(PWM)\}, Q(D)\}. \quad (2) \end{aligned}$$

A controlled PWM with pulsewidth δ is symmetrically generated by the comparisons of the triangle carrier Vc and modulation signal Vm. The rising edge matching of Vc and Vm triggers the polarity inversion of the leading bridge, while the falling edge matching of Vc and Vm triggers the polarity inversion of the lagging bridge. When Vm has a change ΔVm, this modulation simultaneously moves gate1 and gate3 in the opposite direction. Thus, the derived Vab is symmetrical with respect to Vc.

Operation Cycles

Fig. 3 demonstrates the ideal waveforms of proposed inverter. Vc is the triangular carrier, and Vpp is the peak value of Vc. The modulation signals of triangular carrier are Vm 1c, Vm 1b, Vm 2c and Vm 2b . Vm 1b and Vm 2b are used to control phase-shift angles of H-Bridge 1 and HBridge 2, respectively, and δi is the duration of voltage levels controlled by them. Vm 1c and Vm 2c are used to control the alternative operations of SC1 and SC2, respectively, and αi is the duration of voltage levels controlled by them. Thus, the drive signals ofH-Bridge switches (S1a, S1b, S1c, S1d, S2a, S2b, S2c, S2d) are phase-shifted pulse signals, while the drive signals of SC switches (S1, S2, S_1 , S_ 2) are complementary pulse signals. Two operational modes are presented as shown in Fig. 3(a) and (b). Mode 1 is similar to mode 2 apart from the different positions of modulation signals (Vm 1c , Vm 1b , Vm 2c , Vm 2b). Consequently, the durations of each voltage level are controlled by modulation signals in both mode 1 and mode 2.

Active circuits of the operational mode 1 are demonstrated in Fig. 4. Re is the equivalent load. When t satisfies $t0 \leq t < t1$ in Fig. 3(a), the switches S1a, S1b, S2a, S2b are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in freewheeling state, and output voltage equals 0. Because S_1and S_2 are on, the capacitors C1 and C2 are charged to Vin(Vdc1 = Vdc2 = Vin). The voltages on Bus 1 and Bus 2 are Vin as well. The current flow of this time interval is shown in Fig. 4(a). When t satisfies $t1 \leq t < t2$ in Fig. 3(a), the switches S1a, S1b, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridge 1 is in freewheeling state, and HBridge 2 is in positive conducting state. Output voltage equals Vin . Because S_1 and S_2 are on, the capacitors C1 and C2 keep charged to Vin (Vdc1 = Vdc2 = Vin). The voltages on Bus 1 and Bus 2 are Vin as well. The current flow of this time interval is shown in Fig. 4(b). When t satisfies $t2 \leq t < t3$ in Fig. 3(a), the switches S1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. HBridges 1 and 2 are in positive conducting state.Output voltage equals 2Vin . Because S_1 and S_2 are on, the capacitors C1 and C2 keep charged to Vin (Vdc1 = Vdc2 = Vin). The voltages on Bus 1 and Bus 2 are Vin as well.

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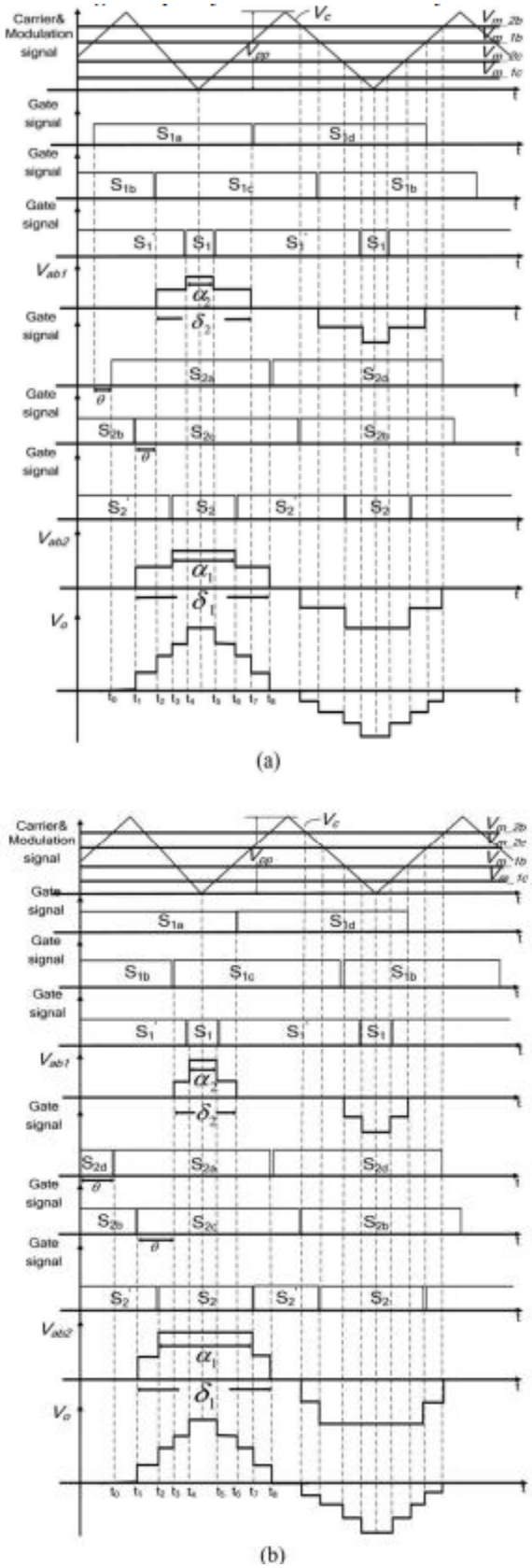
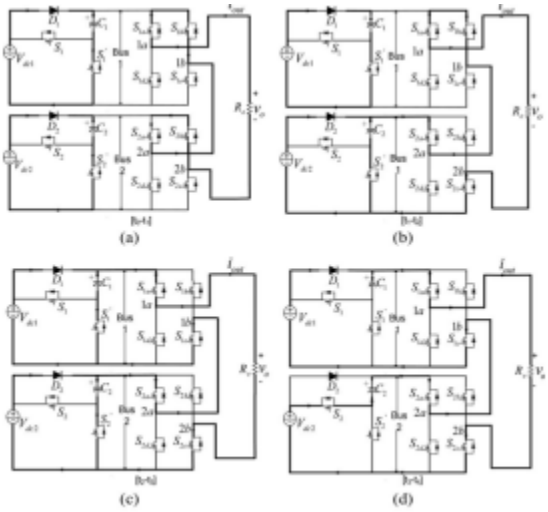


Fig.3. Operational waveforms of the proposed multilevel inverter. (a) Operational mode 1. (b) Operational mode 2.

The current flow of this time interval is shown in Fig. 4(c). When t satisfies t3 ≤ t < t4 in Fig. 3(a), the switches S1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state.Output voltage equals 3Vin . Because S_1 and S2 are on, the capacitor C1 keeps charged to Vin (Vdc1 = Vdc2 = Vin), and the capacitor C2 is discharged. The voltages on Bus 1 and Bus 2 are Vin and 2Vin , respectively. The current flow of this time interval is shown in Fig. 4(d). When t satisfies t4 ≤ t < t5 in Fig. 3(a), the switches S1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals 4Vin . Because S1 and S2 are on, the capacitor C1 and C2 are discharged. The voltages on Bus 1 and Bus 2 both are 2Vin . The current flow of this time interval is shown in Fig. 4(e).



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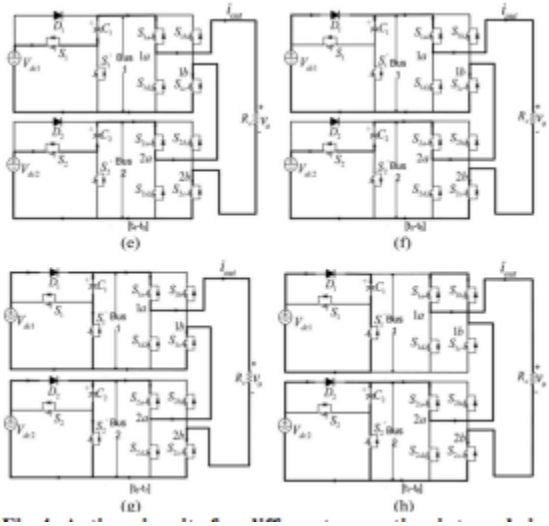

Fig.4. Active circuits for different operation intervals in the operational mode 1: (a) t0 − t1; (b) t1 − t2; (c) t2 − t3; (d) t3 − t4; (e) t4 − t5 ; (f) t5 − t6 ; (g) t6 − t7 ; (h) t7 − t8 .

The operations in t5 ≤ t < t6, t6 ≤ t < t7 , and t7 ≤ t < t8, are the same as the operations in t3 ≤ t < t4, t2 ≤ t < t3 , and t1 ≤ t < t2 , respectively. The active circuits are shown in Fig. 4(f)– (h). Comparing with operational mode 1, the mode 2 has the different active circuits in two time intervals. When t satisfies t2 ≤ t < t3 in operational mode 2 as shown in Fig. 3(b), the switches S1a, S1b, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive conducting state. Output voltage equals 2Vin . Because S_1 and S2 are on, the capacitor C1 keeps charged to Vin and capacitor C2 is discharged. The voltages on Bus 1 and Bus 2 are Vin and 2Vin , respectively. The current flow of this time interval is shown in Fig. 5(a). Similarly, the active circuit of t6 ≤ t < t7 is shown in Fig. 5(b) that has the same operations as t2 ≤ t

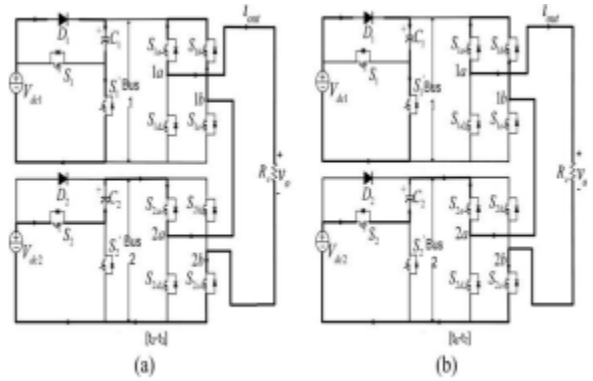

Fig.5. Active circuits for different operation intervals in the operational mode 2: (a) t2 − t3 ; (b) t6 − t7 .

The second half-cycle (from t8 on) has the similar active circuits as the first half-cycle (t1 − t8), but the current will be circulated in the opposite direction to provide the negative output voltage. The relations of on-state switches and output voltage level are described in Table I, as well as operations of two modes are compared closely. Table I has ten working states for nine voltage levels. When the operation enters a new state from an adjacent state, only one power switch changes between on and off. The device stress in switching devices of H-bridge circuit is higher than that in SC circuit. It can also be found that the output voltage in Mode 1 is more stable than Mode 2 due to less discharging period of switching capacitor. Along with the up-down movement of modulation signals (Vm 1c, Vm 1b, Vm 2c, Vm 2b), the output voltage of the proposed inverter is a controllable nine-level staircase. The duration of each voltage level is determined by the duty-cycle of SC circuit and the phase-shifted angle of H-Bridge circuit.

Operation Cycles

In aforementioned nine-level inverter, the staircase output vo can be divided into four components v01, v02, v03, and v04, as shown in Fig. 6. The durations of each component are decided by the comparisons of reference signal (Vm 1c, Vm 1b, Vm 2c, Vm 2b) and triangular carrier (Vc). If pulsewidths of the constituted component are defined as δ1, δ2, α1 , and α2 , Fourier analysis is accomplished for this nine-level staircase. The magnitude of the harmonics is derived by

$$V_n = \frac{4V_{in}}{n\pi}\left(\cos\left(n\left(\frac{\pi-\alpha_1}{2}\right)\right)+\cos\left(n\left(\frac{\pi-\delta_1}{2}\right)\right) + \cos\left(n\left(\frac{\pi-\alpha_2}{2}\right)\right)+\cos\left(n\left(\frac{\pi-\delta_2}{2}\right)\right)\right), \quad n = 1, 3, 5, \ldots \tag{3}$$

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Table I. Relations of On-State Switches and Output Voltage

Mode 1			Mode 2		
On-state switches	Output voltage	Capacitor State	On-state switches	Output voltage	Capacitor State
$S_1, S_2, S_3, S_5, S_7, S_8$	$4V_{in}$	C_1, C_2 Discharging	$S_1, S_2, S_3, S_5, S_7, S_8$	$4V_{in}$	C_1, C_2 Discharging
$S_1, S_2, S_3, S_5, S_7, S_8$	$3V_{in}$	C_2 Discharging	$S_1, S_2, S_3, S_5, S_7, S_8$	$3V_{in}$	C_2 Discharging
$S_1, S_2, S_3, S_5, S_7, S_8$	$2V_{in}$	C_1, C_2 Charging	$S_1, S_2, S_3, S_5, S_7, S_8$	$2V_{in}$	C_2 Discharging
$S_1, S_2, S_3, S_5, S_7, S_8$	V_{in}	C_1, C_2 Charging	$S_1, S_2, S_3, S_5, S_7, S_8$	V_{in}	C_1, C_2 Charging
$S_1, S_2, S_3, S_5, S_7, S_8$ or S_1, S_4, S_5, S_6	0	C_1, C_2 Charging	$S_1, S_2, S_3, S_5, S_7, S_8$ or S_1, S_4, S_5, S_6	0	C_1, C_2 Charging
$S_1, S_4, S_5, S_4, S_7, S_8$	$-V_{in}$	C_1, C_2 Charging	$S_1, S_4, S_5, S_4, S_7, S_8$	$-V_{in}$	C_1, C_2 Charging
$S_1, S_4, S_5, S_4, S_7, S_8$	$-2V_{in}$	C_1, C_2 Charging	$S_1, S_4, S_5, S_4, S_7, S_8$	$-2V_{in}$	C_2 Discharging
$S_1, S_4, S_5, S_4, S_7, S_8$	$-3V_{in}$	C_2 Discharging	$S_1, S_4, S_5, S_4, S_7, S_8$	$-3V_{in}$	C_2 Discharging
$S_1, S_4, S_5, S_4, S_7, S_8$	$-4V_{in}$	C_1, C_2 Discharging	$S_1, S_4, S_5, S_4, S_7, S_8$	$-4V_{in}$	C_1, C_2 Discharging

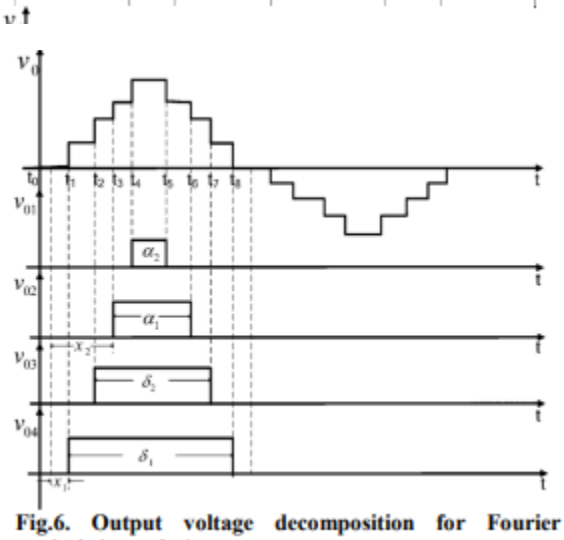

Fig.6. Output voltage decomposition for Fourier analysis in mode 1.

In operational mode 1

$$\delta_1 = \frac{V_{m\_2b}}{V_{pp}}\pi, \qquad \alpha_1 = \frac{V_{m\_1b}}{V_{pp}}\pi,$$
$$\delta_2 = \frac{V_{m\_2c}}{V_{pp}}\pi, \qquad \alpha_2 = \frac{V_{m\_1c}}{V_{pp}}\pi. \tag{4}$$

In operation mode 2

$$\delta_1 = \frac{V_{m\_2b}}{V_{pp}}\pi, \qquad \alpha_1 = \frac{V_{m\_2c}}{V_{pp}}\pi,$$
$$\delta_2 = \frac{V_{m\_1b}}{V_{pp}}\pi, \qquad \alpha_2 = \frac{V_{m\_1c}}{V_{pp}}\pi. \tag{5}$$

To further describe the relations of output THD and pulse widths α1, α2, δ1, δ2 , four parameters are predefined

$$k_1 = \frac{\alpha_1}{\delta_1}, \quad k_2 = \frac{\alpha_2}{\delta_2}, \quad x_1 = \frac{\pi - \delta_1}{2}, \quad x_2 = \frac{\pi - \delta_2}{2}. \tag{6}$$

The output waveforms can be characterized by these four constants. According to the definitions as , THD of output voltage can be calculated by the harmonic magnitudes. The relations of output THD to x1, x2 are given in Fig. 7 with the fixed k1 and k2. It can be found from Fig. 7 that THD is easy to be regulated by the duration width of voltage levels. At the suitable scope of x1 and x2 , THD of output voltage is less than 10%.When k1 = 0.6 and k2 =0.4, THD can be less than 10% within the scope of 0.05 < x1 < 0.5 and 0.4< x2 < 0.6. When k1 = 0.5 and k2 = 0.5, THD can be less than 10% within the scope of 0< x1 < x2 < 0.6. Furthermore, THD becomes less along with the increasing number of voltage levels. The output magnitude of multilevel inverter can be regulated by the duration width of voltage levels as well. Two patterns are available to perform the regulations of THD and magnitude simultaneously. One is to regulate x1, x2 with the fixed k1, k2.

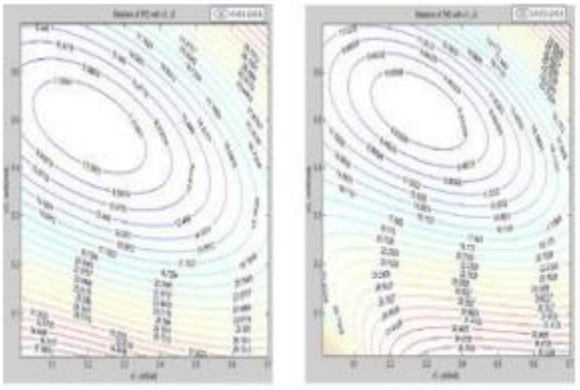

Fig. 7. Relation curves of output THD versus *x*1, *x*2 (unit, rad): (a) *k*1 = 0.6, *k*2 = 0.4; (b) *k*1 = 0.5, *k*2 = 0.5.

The other one is to regulate k1, k2 with the fixed x1, x2 . The numerical benchmark and THD optimization will be examined in the future study, and a fixed ratio (k1 = k2 = 0.5, x1 = π/8, x2 = π/4) is adopted to evaluate output harmonics in subsequent simulation and experiment. If the proposed dc–ac inverter is used as second stage of ac–ac conversion, an ac–dc controlled rectifier is introduced as preceding stage of ac–ac conversion. Power factor correction (PFC) implemented by dc–dc converter can improve the power factor in ac–dc conversion. In this case, both SC and H-bridge generate the optimized pulsewidth to minimize output THD. The magnitude regulation of output voltage can be performed by controllable ac–dc stage in input side. The minimized THD is achieved by this two-stage power circuit, namely, ac–dc stage is used to regulate magnitude, and dc–ac stage formed by the proposed inverter is used to minimize THD.

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Simulation Evaluation

The simulation based on PSIM is performed for the proposed inverter. The waveforms of output voltage vo , capacitor currents (iC1, iC2) and capacitor voltages (vC1, vC2) are shown in Fig. 10. The following parameters are used for low power simulation. The input voltage is Vin = 12 V, the module 1 capacitor is C1 = 100 μF with 80 mΩ ESR, the module 2 capacitor is C2 = 220 μF with 50 mΩ ESR, the diodes D1 and D2 have 0.6 V forward voltage drop and 50 mΩ internal on-state resistance, and the load resistance is Ro = 12 Ω. The following parameters are used for high-power simulation. The input voltage is Vin = 100 V, the module 1 capacitor is C1 = 300 μF with 30 mΩ ESR, the module 2 capacitor is C2 = 560 μF with 20 mΩ ESR, and the load resistance is Ro = 12 Ω. The output frequency fsis 25 kHz.

The waveforms of low power and high power are demonstrated in Fig. 10(a) and (b), respectively. It can be seen that the proposed inverter can work at higher power. C1 and C2 can be converted to resonant switched-capacitor topology easily [29], [30] and hence the less power loss can be achieved in the frontend SC stage. The simulation waveforms are accorded with theoretical analysis. C1 is discharged at the interval of t4 to t5, and C2 is discharged at the interval of t3 to t6 . Both capacitors are charged and discharged once every half cycle. Because of the internal resistance of diodes D1 and D2, the charging current can be divided into several subintervals that are in accordance with operational analysis in Fig. 4. Considering the charging cycle and RC time constant, the peak current of charging period and voltage drop of discharging period are rational at the given conditions. Theoretically, low power can obtain amplitude of 4× 12 V, and high power can obtain amplitude of 4 × 100 V.

However, an amplitude difference emerges between theoretical results and simulation waveforms. In low power simulation, the voltage of the capacitors C1 varies between 11 and 11.3 V, while the voltage of the capacitors C2 varies between 10.8 and 11.1 V. In high power simulation, the voltage of the capacitors C1 varies between 91 and 95 V, while the voltage of the capacitors C2 varies between 89 and 91 V. Thus, the amplitude of simulation waveform is less than the theoretical amplitude caused by forward voltage drop and inner resistance.

The output voltage and voltage spectrum are compared in Fig. 11, including 9- and 13-level inverter. Fig. 11(a) is output waveform of nine-level inverter at condition of k1 = k2 = 0.5, x1 = π/8, and x2 = π/4. The voltage step in staircase output has a slightly drop at t = 0.00465–0.00475 due to the discharging cycle of SC. Fig. 11(c) is output waveform of 13-level inverter with the same duration of each voltage level. A thirteen-level inverter adopts 3 × 2 structure, and the following circuit parameters are used. The input voltage is Vin = 12 V, the module 1 capacitors are C1 = 100 μF C_ 1 = 120 μF with 80 mΩ ESR, the module 2 capacitor are C2 = 220 μF C_ 2 = 250 μF with 50 mΩ ESR, and the load resistance is Ro = 12 Ω.

It can be found from Fig. 11(c) that the voltage drop is indistinctive in each step of staircase output because the discharging periods of SCs become shorter for 13-level inverter. The output spectrums of 9-level and 13-level inverter are illustrated in Fig. 11(b) and (d), respectively. The fundamental frequency is 25 kHz that is the same as output frequency. It can be observed that the fundamental harmonic is significantly higher than the other harmonics. The magnitude of fundamental component is below 40 V for nine-level inverter, while the magnitude of fundamental component is 55 V for a 13-level inverter. The dominating harmonics are compared in Table III.

The calculated THD is 19.1% for 9-level inverter and 14.1% for 13-level inverter. A 13-level inverter has fewer high order harmonics than nine-level inverter. It can be estimated that the harmonics can be further cut down along with the increasing number of voltage levels. Thus, the proposed inverter produces near sinusoidal staircase output, and two methods can make it more sinusoidal. One is to optimize the duration of voltage levels; the other one is to increase the number of voltage levels.

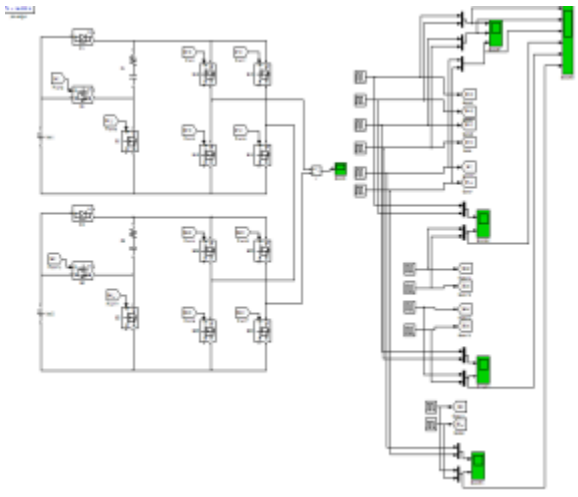

Fig8.. Matlab Simulink model of the proposed Method 9 level multilevel Inverter.

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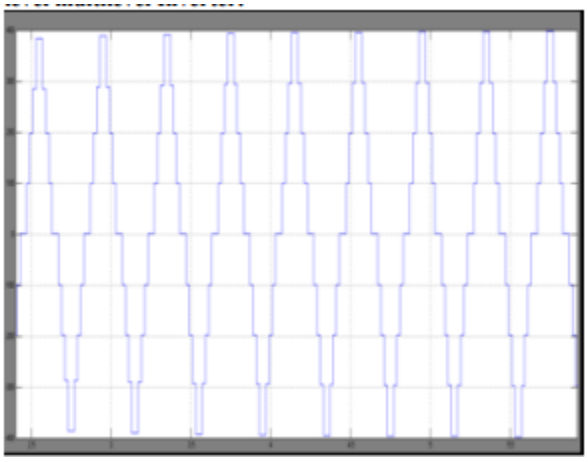

Fig9.Output Voltage of the 9 level inverter

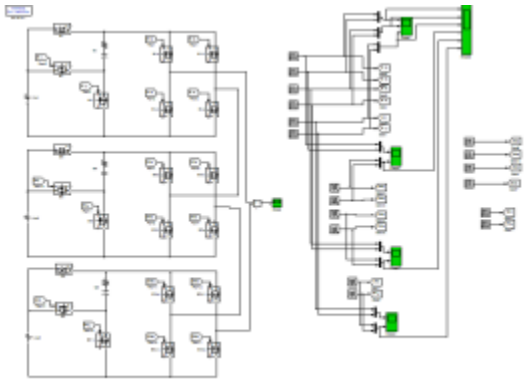

Fig.10. Matlab Simulink model of the proposed Method 13 level multilevel Inverter.

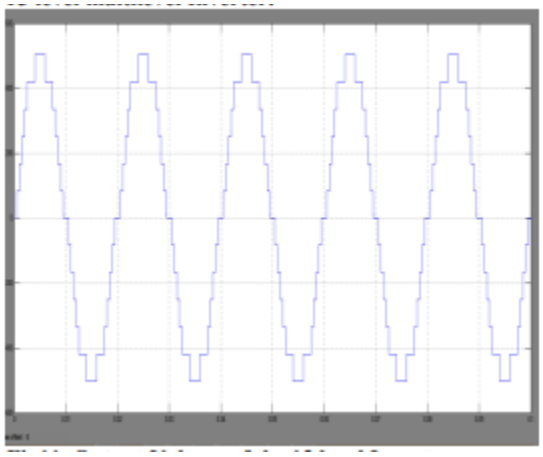

Fig11. Output Voltage of the 13 level Inverter.

IV. CONCLUSION

This research presented a new cascaded multilevel inverter that is based on SC. A thorough analysis is conducted on both the 9-level and 13-level circuit topologies. The number of switching devices needed by the suggested inverter is much less than that of a traditional cascaded multilevel inverter. With a low switching frequency and easy implementation, symmetrical PSM, a single carrier modulation, was introduced. Consistent simulation findings validate the practicability of the suggested circuit and modulation technique. The number of voltage levels may be further enhanced by using a SC frontend compared to a standard cascade H-bridge. Take a 9-level circuit as an example; in half a cycle, the number of voltage levels rises twice; in a 13-level circuit, it grows three times. The suggested multilayer inverter may function as an HF power source with controllable magnitude and fewer harmonics since the magnitude control is achieved by pulsewidth modulation of the voltage level. The focus of this work is on inverters with nine or thirteen levels. All of the components of the proposed inverter may be analyzed and designed using the same process. The suggested inverter is suitable for electric vehicle (EV) electrical networks and grid-connected photovoltaic systems due to the abundance of readily accessible dc sources such as fuel cells, ultra capacitors, solar panels, and batteries.

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