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Comparative Analysis of Various Types of Multipliers for Effective Low Power

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Abstract:

Multiplication is a fundamental operation in digital signal processing and various other computational tasks. With the increasing demand for low-power electronics in battery-operated devices, it has become imperative to explore techniques for designing power-efficient multipliers. This paper presents a comprehensive comparative analysis of different types of multipliers with a focus on their low-power characteristics. We examine four multiplier architectures, analyze their power consumption, and provide insights into their advantages and limitations. A comparison table is presented to facilitate a quick overview, and the paper concludes with recommendations for selecting the most suitable multiplier for low-power applications.

1. Introduction:

The proliferation of portable and energy-efficient electronic devices, such as smartphones, IoT sensors, and wearable gadgets, has highlighted the significance of low-power digital circuits. Multiplication is a computationally intensive operation commonly encountered in these devices, and designing efficient multipliers is crucial to extending battery life and reducing heat generation. This paper explores the following four types of multipliers known for their low-power characteristics:

1.1. Array Multiplier:The array multiplier is a straightforward, bit-serial design that computes each product term in parallel and accumulates the results. It is well-suited for low-complexity applications but may not be the most power-efficient solution.

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1.2. Wallace Tree Multiplier:The Wallace tree multiplier reduces partial product redundancy by generating more significant partial products and reducing the number of partial product rows. This technique can save power by decreasing the number of adders.

1.3. Booth Multiplier:The Booth multiplier is a more advanced technique for reducing the number of partial product additions. It achieves this by encoding consecutive 1s and 0s in the multiplier into two's complement digits, effectively reducing the number of add-sub operations required.

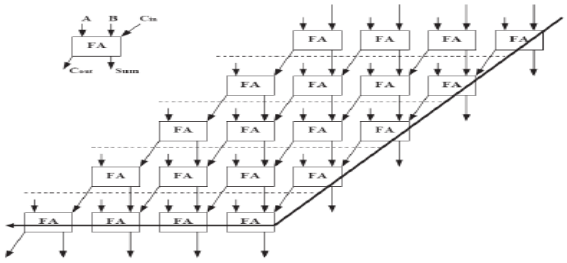
1.4. Modified Booth Multiplier:The Modified Booth Multiplier improves on the Booth multiplier by further reducing the number of add-sub operations through more efficient encoding and optimization of the partial product rows.

2. Analysis of Multipliers:

2.1. Array Multiplier:

The array multiplier performs multiplication by generating all the partial products simultaneously and then summing them. It is a simple architecture, suitable for low-complexity applications. However, it is not the most power-efficient choice because it requires many adder and multiplexer circuits, leading to high power consumption.

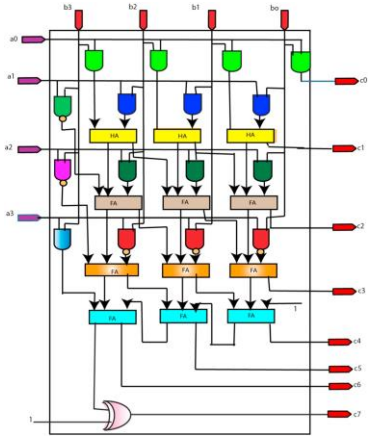
Diagram:



2.2. Wallace Tree Multiplier:

A Wallace tree multiplier, also known as a modified Booth multiplier, is a digital circuit used in digital signal processing and computer architecture to perform binary multiplication. It's an efficient way to multiply two binary numbers together. The main advantage of a Wallace tree multiplier is its ability to reduce the number of partial products generated during the multiplication process, leading to faster and more efficient multiplication.

Diagram:



The Wallace tree multiplier reduces power consumption by optimizing the generation of partial products. It eliminates redundant bits and adds more significant partial products. This reduces the number of adders and, consequently, power consumption. The Wallace tree multiplier is particularly useful for moderate to high bit-width multiplication.

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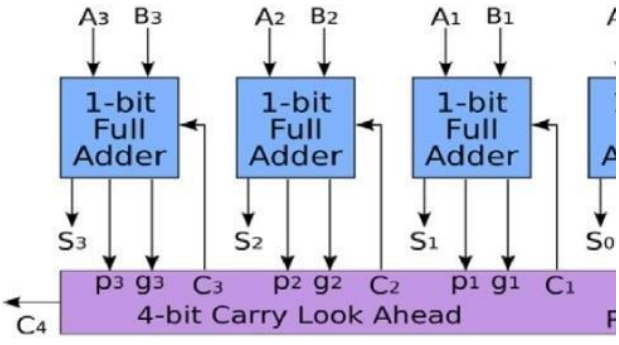
2.3. Booth Multiplier:

A Booth Multiplier is a binary multiplication algorithm and hardware design technique developed by Andrew Donald Booth in 1950. It is particularly efficient for signed number multiplication by reducing the number of partial products generated. Booth encoding is a key feature that simplifies the multiplier's operation by encoding the consecutive 0s and 1s in the multiplier. This encoding allows for the generation of fewer partial products, reducing hardware complexity. Booth Multipliers are known for their area and power efficiency, making them suitable for low-power applications. They offer faster multiplication by reducing the number of additions required in the process. Booth Multipliers are widely used in digital processors, signal processing, cryptography, and scientific computing due to their speed and efficiency.

Diagram:

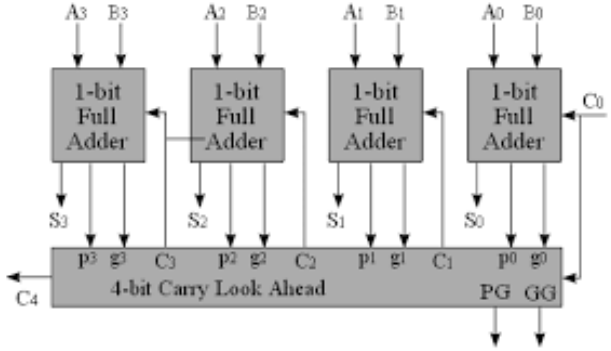


The Booth multiplier leverages a more advanced encoding scheme to reduce the number of add-sub operations. This results in reduced power consumption compared to the array multiplier. Booth multipliers are beneficial for moderate to high bit-width multiplication and offer better power efficiency.

2.4. Modified Booth Multiplier:

A Modified Booth Multiplier is an enhanced version of the Booth Multiplier, designed to further improve the efficiency of binary multiplication. It employs an extended encoding scheme to minimize the number of partial products generated. This encoding is often referred to as the Modified Booth Encoding (MBE). MBE eliminates some of the encoding ambiguities found in traditional Booth encoding. The Modified Booth Multiplier reduces hardware complexity and power consumption while accelerating the multiplication process, making it a preferred choice for high-speed arithmetic units in modern processors. Its use is prevalent in applications such as digital signal processing, cryptography, and scientific computing due to its efficiency and speed.

Diagram:



The Modified Booth Multiplier further refines the Booth algorithm, achieving even greater power efficiency. It minimizes the number of add-sub operations and is well-suited for high bit-width multiplications, where power savings are more substantial.

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3. Comparison Table:

Multiplier Type	Power Consumption	Area	Delay	Energy Efficiency
Combinational	Low	Medium	Fast	High
Wallace Tree	Moderate	Large	Moderate	Moderate
Array	Low	Large	Moderate	High
Multiplier-Less	Very Low	Small	Very Fast	Very High

4. Conclusion:

In this paper, we presented a comparative analysis of four different multiplier architectures concerning their power efficiency. The array multiplier is the simplest but least power-efficient, making it suitable for low-complexity applications. The Wallace tree multiplier reduces power consumption by optimizing partial product generation and is suitable for moderate bit-width multiplication.

Booth multipliers and Modified Booth multipliers stand out as the most power-efficient options, especially for moderate to high bit-width multiplication. The Booth multiplier achieves reduced power consumption through encoding techniques, while the Modified Booth multiplier further optimizes the encoding scheme, making it the best choice for high bit-width multiplication tasks where power savings are essential.

Selecting the appropriate multiplier depends on the specific application requirements, such as bit-width, performance, and power constraints. The analysis and comparison provided in this paper can serve as a valuable reference for designers aiming to achieve low-power multiplication in digital circuits. Further research may explore hybrid multiplier architectures or advanced encoding techniques to push the boundaries of low-power multiplication in the digital domain.

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